REMARKS

Claim 9 is amended. Claims 34 and 35 are added. Claims 9, 10, 13, and 32-35 are pending in the application.

Claims 9, 10, 13, 32 and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsukamoto, U.S. Patent No. 5,700,349 in view of one of Wu, U.S. Patent No. 5,915,182; Wu, U.S. Patent No. 6,107,149; and Ju, U.S. Patent No. 6,232,166. The Examiner is reminded by direction to MPEP § 2143 that a proper obviousness rejection has the following three requirements: 1) there must be some suggestion or motivation to modify or combine reference teachings; 2) there must be a reasonable expectation of success; and 3) the combined references must teach or suggest all of the claim limitations. Claims 9, 10, 13, 32 and 33 are allowable over Tsukamoto as combined with any of Wu '182, Wu '149 and Ju for at least the reason that the references, individually or as combined, fail to disclose or suggest each and every limitation in any of those claims.

As amended independent claim 9 recites forming an electrically insulative material spacer comprising at least two separate layers along a transistor gate sidewall, the first of the at least two layers comprising Al_pO_q where p and q are each greater than 0 and less than 10, and a second of the at least two layers consisting essentially of silicon and nitrogen, the first of the at least two layers being disposed between the transistor gate sidewall and the second of the at least two layers. Claim 9 additionally recites depositing a barrier layer over the spacer and forming a doped oxide layer over the barrier layer. The amendment to claim 9 is supported by the specification at, for example, page 6, lines 12-16 and page 11, lines 8-20.

Tsukamoto discloses forming sidewalls 7, forming an etch stop layer 9 over the sidewalls, and forming an interlayer insulating film 10 (BPSG) directly over the etch stop layer 9 (col. 7, ll. 22-51). Tsukamoto does not disclose or suggest the claim 9 recited depositing a barrier layer over a spacer comprising Al_pO_q and forming a doped oxide layer over the barrier layer. Not one of Wu '182, Wu '149 and Ju disclose or suggest the recited depositing a barrier layer over a spacer comprising Al_pO_q, or the recited forming a doped oxide layer. Accordingly, as combined with Tsukamoto, none of the additionally recited references contributes towards suggesting the claim 9 recited depositing a barrier layer over a spacer and forming a doped oxide layer over the barrier layer, the spacer comprising a first layer of Al_pO_q which is disposed between a transistor gate sidewall and a second layer consisting essentially of silicon and nitrogen. Accordingly, independent claim 9 is not rendered obvious by the cited combinations of Tsukamoto, Wu '182, Wu '149 and Ju, and is allowable over these references.

Dependent claims 10, 13, 32 and 33 are allowable over the cited combinations of Tsukamoto, Wu '182, Wu '149 and Ju for at least the reason that they depend from allowable base claim 9.

New claims 34 and 35 do not add "new matter" to the application since each is fully supported by the specification as originally filed. Claims 34 and 35 are supported by the specification at, for example, page 6, lines 12-16; and page 11, lines 8-20.

For the reasons discussed above claims 9, 10, 13, 32 and 33 are allowable, and claims 34 and 35 are believed allowable. Accordingly, applicant respectfully requests formal allowance of pending claims 9, 10, 13 and 32-35 in the Examiner's next action.

Respectfully submitted,

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By: Jennifer J. Taylor
Jennifer J. Taylor, Ph.D.
Reg. No. 48,711